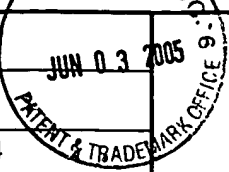


First Named Inventor	Leonard Forbes		INFORMATION DISCLOSURE STATEMENT
Serial No.	10/808,059		
Filing Date	March 24, 2004		
Group Art Unit	2814		
Examiner Name	Marcos D. Pizarro Crespo		
Confirmation No.	4221		
Attorney Docket No.	400.285US01		
Title: NROM MEMORY DEVICE WITH HIGH-PERMITTIVITY GATE DIELECTRIC FORMED BY THE LOW TEMPERATURE OXIDIZATION OF METALS			

Mail Stop: AMENDMENT
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

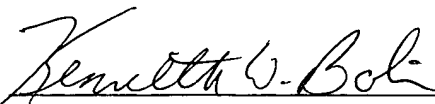
In compliance with 37 C.F.R. §§ 1.56 and 1.97, *et seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified Application. Pursuant to 37 C.F.R. 1.98 (a)(2)(i), as this application was filed after June 30, 2003, Applicant has not included copies of U.S. Patents or U.S. Patent Applications. Applicant respectfully requests that this Information Disclosure Statement be entered and the references listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to MPEP §609, Applicant further requests that the Examiner initial next to each reference on the Form 1449 to indicate that the listed references have been considered. Applicant further requests that a copy of the initialed Form 1449 be returned with the next official communication.

As an Office Action has not yet issued in this application, Applicant believes that no fees are due. However, the Commissioner for Patents is hereby authorized to charge any additional fees to Deposit Account No. 501373.

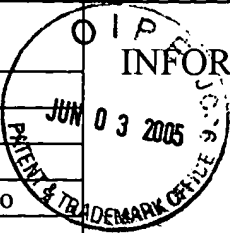
If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211.

Respectfully submitted,

Date: 5/31/05


 Kenneth W. Bolvin
 Reg. No. 34,125

Attorneys for Applicant
 Leffert Jay & Polglaze
 P.O. Box 581009
 Minneapolis, MN 55458-1009
 T 612 312-2200
 F 612 312-2250

First Named Inventor	Leonard Forbes	 <p>INFORMATION DISCLOSURE STATEMENT FORM PTO-1449</p>
Serial No.	10/808,059	
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Sheet 1 of 1		

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Examiner Initials	Foreign Patent		Name	Publication Date	Translation
	Country	No.			

Other References	
Examiner Initials	Author, Title, Date, Pages, etc.
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	Sugizali et al., <i>19th IEEE Non-Volatile Semiconductor Memory Workshop 2003</i> , p. 60-61, "New 2-bit/Tr MONOS Type Flash Memory using..."
	Shin et al., <i>19th IEEE Non-Volatile Semiconductor Memory Workshop 2003</i> , p. 58-59, "High Reliable SONOS-type NAND Flash Memory Cell with Al ₂ O ₃ for Top Oxide"
	Blomme et al., <i>19th IEEE Non-Volatile Semiconductor Memory Workshop 2003</i> , p. 93-94, "A Novel Low Voltage Memory Device with an Engineered SiO ₂ /high-k tunneling barrier"
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	Eitan et al., (November) 2000, <i>IEEE Electron Device Letters</i> , Volume 21, No. 11, p. 543-545, "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell"
	Lusky et al., (November) 2001, <i>IEEE Electron Device Letters</i> , Volume 22, No. 11, p. 556-558, "Characterization of Channel Hot Electron Injection by the Subthreshold Slope..."

Examiner Signature		Date Considered	
*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			